

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

PATENT APPLICATION

Inventors: Douglas J. Tweet, Sheng Teng Hsu,
and Jer-Shen Maa

Attorney Docket No.
SLA0586

Serial No: Not Yet Assigned

Filed: Herewith

Title: METHOD TO FORM LOCAL
SILICON-ON-NOTHING OR
SILICON-ON-INSULATOR WAFERS
WITH TENSILE-STRAINED SILICON

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

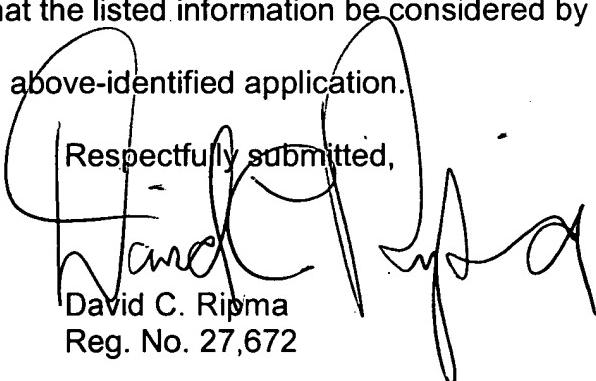
INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Sir:

Listed on attached Form PTO-1449 is information submitted pursuant to
37 C.F.R. §1.56. A copy of each listed publication is submitted herewith.

Applicant respectfully requests that the listed information be considered by
the Examiner and made of record in the above-identified application.

March 23, 2004
(Date)

Respectfully submitted,

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1449A/PTO Rev. 10/95		U.S. Department of Commerce Patent and Trademark Office		Complete If Known	
LIST OF PRIOR ART CITED BY APPLICANT (use as many sheets as necessary)		Application Number			
		Filing Date		03-23-04	
		First Named Inventor		Douglas James Tweet	
		Group Art Unit			
		Examiner Name			
Sheet	1	of	1	Attorney Docket No.	SLA.0586

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, country where published, source.		
		HARRISON ET AL., <i>Highly performant double gate MOSFET realized with SON process</i> , IEDM 03-449, p18.6.1 (2003)		
		YIN, ET AL., <i>Strain relaxation of SiGe islands on compliant oxides</i> , J. Appl. Phys. 91, p. 9716 (2002).		
		R. CHAU ET AL., <i>A 50nm Depleted-Substrate CMOS Transistor</i> , IEDM, p. 621, 2001.		
		TEZUKA ET AL., <i>A Novel Fabrication Technique of Ultrathin and Relaxed SiGe Buffer Layers with High Ge Fraction for Sub-100nm Strained Silicon-on-Insulator MOSFETs</i> , Jpn. J. Appl. Phys. 40, p. 2866 (2001)		
		M. JURCZAK, ET AL., <i>Silicon-on-Nothing (SON) - an innovative Process for Advanced CMOS</i> , IEEE Trans. El. Dev. Vol. 47, pp2179-2187 (2000).		
		MIZUNO ET AL., <i>Advanced SOI-MOSFETs with strained-Si channel for high speed CMOS - electron/hole mobility enhancements</i> , 2000 Symposium on VLSI, p. 210.		
		TRINKAUS ET AL., <i>Strain relaxation mechanism for hydrogen-implanted Si_{1-x}Ge_x/Si (100) heterostructures</i> , Appl. Phys. Lett., 76, p. 3552, (2000).		
		M. JURCZAK ET AL., <i>SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era</i> , VLSI Tech. Dig., p.29, (1999).		
		R. KOH, <i>Buried Layer Engineering to Reduce the Drain-Induced Barrier Lowering of Sub-0.05um SOI-MOSFET</i> Jpn. J. Appl. Phys., Vol. 38, P. 2294 (1999)		
		MANTL ET AL., <i>Strain relaxation of epitaxial SiGe layers on Si (100) improved by hydrogen implantation</i> , Nuclear Instruments and Methods in Physics Research B 147, p. 29, (1999)		
		PAUL, <i>Silicon germanium heterostructures in electronics: the present and the future</i> , Thin Solid Films, 321, p. 172 (1998)		
		RIM ET AL., <i>Transconductance enhancement in deep submicron strained-Si n-MOSFETs</i> , IEDM Proc. p. 707 (1998)		
		WELSER ET AL., <i>Electron mobility enhancement in strained-Si N-type metal-oxide-semiconductor field-effect transistors</i> , IEEE EDL-15, #3, p.100, (1994)		
		RIM ET AL., <i>Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs</i> , IEDM Proc. p. 517 (1995)		

Examiner Signature		Date Considered	
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Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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